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 Ong, A.; Benyamin, S.; Cancio, J.; Conditto, V.; Labrie, T.; Qinghung Lee; Matti D.K.; Shahani, A.; Xiaomin Si; Hai Tao; Tarsia, M.; Wong, W.; Min Xu;
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[AbstractPlus](#) | Full Text: [PDF](#)(1583 KB) IEEE JNL
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- ☐ 2. **Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplan cell**
 Zerbe, J.L.; Werner, C.W.; Stojanovic, V.; Chen, F.; Wei, J.; Tsang, G.; Kim, D W.F.; Ho, A.; Thrush, T.P.; Kollipara, R.T.; Horowitz, M.A.; Donnelly, K.S.;
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- ☐ 3. **A 10-GB/s SONET-compliant CMOS transceiver with low crosstalk and in**
 Werker, H.; Mechnig, S.; Holuigue, C.; Ebner, C.; Mitteregger, G.; Romani, E.; T.; Moyal, M.; Vena, M.; Melodia, A.; Fisher, J.; de Mercey, G.L.G.; Geib, H.;
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- ☒ 4. **Clock and data recovery with adaptive loop gain for spread spectrum Ser**
 Ming-ta Hsieh; Sobelman, G.E.;
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- ☒ 5. **A low jitter, low power, CMOS 1.25-3.125Gbps transceiver**

- ☐ Younis, A.; Boecker, C.; Hossain, K.; Abughazaleh, F.; Das, B.; Yiqin Chen; Re S.; Grung, B.;
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- ☐ 6. **A 10Gb/s/ch 50mW 120/spl times/130/spl mu/m/sup 2/ clock and data rec**
Kaeriyama, S.; Mizuno, M.;
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2003 Page(s):70 - 478 vol.1
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- ☐ 7. **Architecture and methodology of a SoPC with 3.25Gbps CDR based SERI**
dynamic phase alignment
Venkata, R.; Wong, W.; Tran, T.; Chan, V.; Hoang, T.; Lui, H.; Ton, B.; Shumu
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- ☐ 8. **A 62.5 Gb/s multi-standard SerDes IC**
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- ☐ 9. **A UTMI-compatible physical-layer USB2.0 transceiver chip**
Nam, J.-J.; Kim, Y.-J.; Choi, K.-H.; Park, H.-J.;
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- ☒ 10. **A compact phase interpolator for 3.125G Serdes application**
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- ☐ 11. **Effects of amplitude modulation in jitter tolerance measurements of comm**
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Shuguang Li; Junyan Ren; Lianxing Yang; Fan Ye; Zhang, Y.M.M.;
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- ☐ **14. Digital serial communication device testing and its implications on autonomous equipment architecture**
Cai, Y.; Warwick, T.P.; Rane, S.G.; Masserrat, E.;
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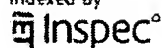
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- ☐ 2. A UTMI-compatible physical-layer USB2.0 transceiver chip
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